Abstract

The present invention relates to a ferroelectric memory device comprising a cell array block, a data bus unit and a control circuit unit. The cell array block has a bitline structure including a main bitline and a plurlaity of sub bitlines. The main bitline is connected to a column selection controller, and the plurality of sub-bitlines have both terminals connected to the main bitline, respectively, and connected to a plurality of unit cells. The data bus unit is connected to the column selection controller. The control circuit unit includes a sense amplifier array connected between a data I/O buffer and a sense amplifier data bus connected to the data bus unit. A plurality of the cell array blocks are arranged like a matrix. The control circuit unit is disposed in a first center line of symmetry wherein the first center line is parallel to the main bitline, and the data bus unit is disposed in a second center line of symmetry wherein the second center line is vertical to the main bitline.

The layout of the disclosed memory device allows capacitance load of a data bus to be minimized in a highly integrated circuit, thereby embodying a high-speed FRAM .